REMARKS

I. Summary of the Examiner's Action

A. Claim Rejections

As set forth in paragraph 3 of the Office Action, claims 1, 2, 5, 6 and 8 stand rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent No. 6,424,178 B1 to Harrison (hereinafter "the Harrison patent").

As set forth in paragraph 4 of the Office Action, claims 3 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Harrison patent and further in view United States Patent No. 6,263,192 B1 to Alderton (hereinafter "the Alderton patent").

These rejections are respectfully disagreed with, and are traversed below.

B. Claim Objections and Allowable Subject Matter

As set forth at paragraph 5 of the Office Action, the Examiner objected to claim 4 as being dependent upon a rejected base claim, but indicated that it would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

II. Applicant's Response – Claim Rejections

A. Rejection of Claims 1, 2, 5, 6 and 8 under 35 U.S.C. § 103(a)

Claim 1 recites the following subject matter:

> 1. A circuit for controlling the duty cycle and jitter of a clock signal, comprising:
>
> an input node for receiving the clock signal; and
>
> an output node for outputting a processed clock signal having a first edge that is synchronized to an edge of the clock signal and a second edge that is varied so as to provide a predetermined processed clock signal duty cycle.

Applicant respectfully submits that it is not seen where the Harrison patent either describes or suggests the subject matter of claim 1.

In particular, claim 1 recites "a circuit ... comprising ... an output node for outputting a processed clock signal having a first edge that is *synchronized* to an edge of the clock signal ..." Harrison is not seen to disclose a circuit that *synchronizes* an edge of a processed clock signal to an edge of an input clock signal. Rather, Harrison necessarily introduces a delay between the edge of the input clock signal and the corresponding edge of the output clock signal because the operations are controlled by the charge and discharge of capacitors. Accordingly, it is not surprising that Harrison nowhere uses the words *synchronize* or *synchronized* either *in haec verba* or

synonymously. "Synchronized" means happening at the same time. One skilled in the art would understand that in a practical circuit like that depicted in FIG. 2 of the instant Application, "synchronized" would mean within a minor propagation delay. Nonetheless, *synchronized* would not describe a system where an intentional delay is introduced between the controlling edge of the input clock signal and the controlled edge of the output clock signal. In such a situation, the corresponding edges of the input and output clock signals are not *synchronized* but rather the controlled edge occurs after an intentional *delay* introduced by the capacitive circuits used by Harrison. In view of the practical operation of Harrison's apparatus, one skilled in the art would expect that *delay* would be used to describe the relative timing of the signals and not *synchronized.*

A review of Harrison's summary of his purported invention confirms this expectation as is apparent from the following portion appearing at column 1, line 60 – column, 2 line 6 reproduced here (emphasis added):

> "A method and system for generating an output clock signal having a controllable duty cycle from an input clock signal in accordance with the invention includes a duty cycle corrector circuit coupled to a duty cycle indicating circuit through a control circuit. The duty cycle corrector circuit is structured to transition the output signal to a first logic level responsive to a first transition of the input clock signal after a first delay that corresponds to a first control signal. The duty cycle corrector circuit is also structured to further transition the output clock signal to a second logic level that is different from the first logic level responsive to a second transition of the input clock signal that is different from the first

> transition of the input clock signal after a second delay that corresponds to a second control signal."

Rather than seeking to synchronize an edge of the output clock signal with an edge of the input clock signal as in the case of Applicant's invention, the Harrison patent discloses methods and apparatus that purposely introduce delays between the controlling edges of the input clock signal and the controlled edges of the output clock signal. So it simply is not seen that an edge of the output clock signal is *synchronized* with an edge of the input clock signal.

This is made even more evident by the description of the operation of Harrison's circuit:

> "The operation of the duty cycle adjustment circuit 12 will now be summarized with reference to the timing diagram of FIG. 3. As shown therein, the CLK-IN signal has a duty cycle that is substantially greater than 50%. When the CLK-IN signal transitions high at time 815 ns, the NMOS transistor 30 turns ON, thereby discharging the capacitor 40 through the NMOS transistors 30, 32. At time 832ns, when the voltage V_c on the capacitor has been discharged to the lower transition voltage of the inverter 42, the output of the inverter 42 transitions high, thereby causing the CLK-OUT signal to transition low, as shown in FIG. 3. The low-to-high transition of the inverter 42 output also turns ON the NMOS positive feedback transistor 48, thereby quickly discharging the capacitor 40. As a result, the voltage V_c on the capacitor 40 reaches ground potential and is maintained there well before the CLK-IN signal transitions low at time 850 ns.

> When the CLK-IN signal transitions low at time 850 ns, the PMOS transistor 20 turns ON, thereby charging the capacitor 40 through the PMOS transistors 20, 22. At time 857 ns, when the voltage V_c on the capacitor 40 has been charged to the higher transition voltage of the inverter 42, the output of the inverter 42 transitions low, thereby causing the CLK-OUT signal to transition high. The PMOS positive feedback transistor 46 is also turned on at this time, thereby quickly charging the capacitor 40. As a result, the voltage V_c on the capacitor 40 reaches the supply voltage V_{cc} and is maintained there until the CLK-IN signal transitions high at time 865 ns."

As is seen from this description, the Harrison apparatus introduces a controlled delay between the controlling edges of the input clock signal and the controlled edges of the output clock signal. Accordingly, it is not seen where Harrison either describes or suggests *synchronized* operation.

For the foregoing reasons, Applicant respectfully submits that claim 1 is patentable over the Harrison patent. Applicant therefore respectfully requests that the Examiner withdraw the rejection of claim 1. Applicant respectfully submits that independent claim 5 is patentable for reasons similar to claim 1 and for reasons attributable to its independently-recited features. Accordingly, Applicant respectfully requests that the rejection of claim 5 be withdrawn as well. Dependent claims 2, 6 and 8 are patentable both as depending from allowable base claims and for reasons attributable to their independently-recited features. As a result, Applicant also respectfully requests that the rejection of claims 2, 6 and 8 be withdrawn.

B. Rejection of Claims 3 and 7 under 35 U.S.C. § 103(a)

Applicant respectfully submits that Alderton is not seen to remedy the defiencies identified above with respect to the Harrison patent. Accordingly, claims 3 and 7 are patentable both as depending directly on allowable base claims and for reasons attributable to their independently-recited features. For these reasons, Applicant respectfully request that the rejection of claim 3 and 7 be withdrawn.

III. Conclusion

The Applicant submits that in light of the foregoing remarks the application is now in condition for allowance. Applicant therefore respectfully requests that the outstanding rejections be withdrawn and that the case be passed to issuance.

Respectfully submitted,

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